IFW AF/2815

PTO/SB/21 (08-03)
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		Application Number	09/492,243
		Filing Date	Jan 27, 2000
		First Named Inventor	He, Yue-Song
		Art Unit	2815
		Examiner Name	Ortiz, E.
Total Number of Pages in This Submission	54	Attorney Docket Number	0180130 (Previously M-7469-US)

ENCLOSURES *(check all that apply)*

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  - [X] Fee Attached
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  - [ ] Affidavits/declaration(s)
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Remarks

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Firm or Individual name	Michael Farjami, Esq., Reg. No. 38,135 Farjami & Farjami LLP
Signature	
Date	April 27, 2004

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/492,243
Filing Date	1/27/2000
First Named Inventor	He, et al.
Examiner Name	Ortiz, E.
Art Unit	2815
Attorney Docket No.	0180130 (Previously M-7469-US)

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	-20**=		X		=	
Independent Claims	- 3**=		X		=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

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1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)330.00

SUBMITTED BY

Complete *(if applicable)*

Name (Print/Type)	Michael Farjami, Esq.	Registration No. (Attorney/Agent)	38135	Telephone	(949) 282-1000
Signature				Date	4/27/04

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Art Unit: 2815
He, et al.	Examiner: Ortiz, Edgardo
Serial No.: 09/492,243	
Filed: January 27, 2000	
For: **Method And Apparatus For Improved Performance Of Flash Memory Cell Devices**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 3, 4, 9, and 12-14. The Final Rejection issued on September 29, 2003. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on February 27, 2004.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 3, 4, 9, and 12-14 are pending, and claims 1-2 and 10-11 were canceled and claims 5-8 were withdrawn in previous amendments. Claims 3, 4, 9, and 12-14 have been finally rejected in a Final Rejection dated September 29, 2003. This Appeal is directed to the rejection of claims 3, 4, 9, and 12-14. Claims 3, 4, 9, and 12-14 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments were submitted on January 15, 2004 in response to the Final Rejection dated September 29, 2003.

SUMMARY OF INVENTION

A. Claim 3 and its dependent claim

The present invention, as defined by independent claim 3, includes a plurality of series-connected floating gate transistors, where each floating gate transistor has a source

and a drain region formed in a well of a substrate, a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type.

As disclosed in the present application, NMOS transistors 14, 16, and 18, which include respective floating gates 56m1, 56m2, and 56m3, are formed in P type well 32 of substrate 30 and are interconnected in series along a bit line by source/drain regions 62 and 64. Page 4, lines 30-34, page 5, line 1, page 6, lines 13-14, and Figure 2 of the present application. As disclosed in the present application, a retrograde distribution of dopant, which can be accomplished, for example, by implanting an N type dopant at a tilt angle of 45° to vertical, is introduced into channel regions 72, 74, and 76 of respective NMOS transistors 14, 16, and 18 at region 80. Page 6, lines 15-21, page 7, lines 1-7, and Figure 2 of the present application.

As further disclosed in the present application, "after an annealing step, region 80 has a dopant distribution that increases from the level in the substrate closest to the tunnel oxide 52 to the level of the target area and then decreases down through the substrate." Page 7, lines 8-12 of the present application. Additionally, "region 80 has a lateral distribution which tends to be highest toward the centerline axis, and decreases in the direction toward opposing source/drain regions." Page 7, lines 12-15 of the present

application. For example, region 80 decreases toward source/drain regions 60 and 62 for NMOS transistor 14 and decreases toward source/drain regions 62 and 64 for NMOS transistor 16. Page 7, lines 16-17 of the present application. Thus, the present invention provides a non-uniform concentration of dopant in the channel regions, i.e. channel regions 72, 74, and 76 of respective NMOS transistors 14, 16, and 18.

As a result, the invention provides a retrograde dopant distribution in the channel that provides additional carriers, such as electrons in the case of an NMOS device, in the channel and decreases the series channel resistance such that transistors 14, 16, and 18 operate in a manner similar to NMOS buried channel devices. Page 7, lines 18-23 of the present application. By providing a retrograde dopant distribution in the channel that provides additional carriers in the channel and, consequently, reduces series channel resistance, the present invention advantageously allows source/drain dopant levels to be reduced in order to combat short channel effects. Page 12, lines 26-29 of the present application. Thus, for an NMOS transistor, such as NMOS transistors 14, 16, and 18, the present invention provides a non-uniform concentration of dopant that provides additional electrons in the channel and, consequently, has N type conductivity, which is the same conductivity type as source/drain regions, such as source/drain regions 62, 64, and 66. Furthermore, by decreasing the series resistance in the bit line, the invention advantageously provides higher output current that is available for sensing for a given selected Vcc. Page 3, lines 15-17 of the present application.

Dependent claim 4 specifies an embodiment of the memory array of independent claim 3 wherein a dopant concentration region, such as region 80, is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of each floating gate transistor, such as floating gate NMOS transistors 14, 16, and 18. For example, the retrograde distribution of dopant can be accomplished by implanting an n-type dopant at a tilt implant angle of 45° to vertical. Page 6, lines 18-21 of the present application.

B. Claim 9 and its dependent claims

The present invention, as defined by independent claim 9, includes a transistor having a source and a drain region formed in a well of a substrate, where a channel region separates the source and drain regions, a dopant concentration region displaced about a target region situated below the channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. The present invention, as defined by independent claim 9, includes a transistor, such as transistor 14, 16, or 18 in Figure 2 of the present application, having a similar dopant concentration region, i.e. region 80 in Figure 2, as discussed above in relation to independent claim 3. Thus, the invention as defined by independent claim 9 provides similar advantages as the present invention as defined by independent claim 3 discussed above.

Dependent claims 12-14 specify various embodiments of the transistor of independent claim 9. Thus, claim 12 specifies the transistor of independent claim 9 having a dopant concentration region, such as region 80, that is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of the transistor. Dependent claim 13 further specifies the transistor of independent claim 9 as being an NMOS transistor, and dependent claim 14 further specifies the NMOS transistor of dependent claim 13 as being a floating gate transistor.

ISSUE

Whether the Examiner's rejection that claims 3, 4, 9, and 12-14 on Appeal are unpatentable under 35 U.S.C. §103 over U.S. Patent No. 5,894,146 to Pio et al. ("Pio") in view of U.S. Patent No. 5,547,882 to Juang et al. ("Juang") is erroneous.

GROUPING OF CLAIMS

Claims 3 and 4 stand or fall together and, separately, claims 9 and 12-14 stand or fall together, for the reasons set forth in the Argument.

ARGUMENT

A. Claims 3 and 4

Claims 3-4 stand rejected under 35 U.S.C. §103 over Pio in view of Juang. For the reasons discussed below, Appellant respectfully submits that the present invention, as

defined by independent claim 3, is patentably distinguishable over Pio and Juang, considered singly or in combination thereof.

In contrast to the present invention as defined by independent claim 3, Pio and Juang do not teach, disclose, or suggest a plurality of series-connected floating gate transistors, where each floating gate transistor has a source and a drain region formed in a well of a substrate, a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. Pio specifically discloses a matrix comprising a number of memory cells, where each cell 1 includes transistor 2, which is a floating gate transistor, in series with transistor 3, which is a selection MOS transistor. See, for example, column 4, lines 2-7 and 17-19 and Figures 1 and 8 of Pio. In Pio, cell 1 includes source and drain regions 15 and 16, where source region 15 is situated in a well (designed by "p-" in Figure 8) and drain region 16 is situated in the substrate (designated by "p" in Figure 8). See, for example, column 5, lines 52-57 and Figure 8 of Pio.

Thus, in Pio, only source region 15 is situated in a well, not source region 15 and drain region 16 as stated by the Examiner on page 2 of the Final Rejection dated September 29, 2003. Furthermore, Pio fails to teach, disclose, or suggest a plurality of floating gate transistors connected in series, where each floating gate transistor has a source and a drain region formed in a well. Additionally, in Pio, transistor 2 (e.g. a

floating gate transistor) is connected in series with transistor 3, which is a selection MOS transistor and not a floating gate transistor. Moreover, Pio fails to teach, disclose, or suggest a memory array comprising a plurality of floating gate transistors connected in series, as specified in independent claim 3.

Furthermore, Pio fails to teach, disclose, or suggest a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. Moreover, Pio fails to provide any motivation for forming a dopant concentration region displaced about a target region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the source and drain regions and the dopant concentration region have a second conductivity type.

Thus, Pio has failed to disclose a memory array comprising a plurality of floating gate transistors connected in series and a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type, which are also not disclosed or suggested in Juang.

Juang discloses a method for improving punch-through immunity in a semiconductor device by forming a retrograde channel profile by implanting phosphorus ions through a polysilicon gate. See, for example, Juang, column 2, lines 32-36. Juang specifically discloses implanting boron ions into silicon substrate 30 to adjust the threshold of the semiconductor device. See, for example, column 2, lines 50-53 and Figure 4 of Juang. In Juang, phosphorus ions are implanted through gate 62 into channel 66 to achieve a retrograde channel profile as well as to obtain proper threshold voltage. See, for example, column 3, lines 2-6 and Figure 6 of Juang. In Juang, retrograde channel profile curve 73 is achieved by implanting phosphorus ions in channel 66 to neutralize part of the boron ions that have been previously implanted in channel 66, where the concentration of phosphorus ions is smaller than the concentration of boron ions. See, for example, column 3, lines 24-28 and Figure 7 of Juang.

Thus, in Juang, since the concentration of phosphorus ions, which have N type conductivity, is smaller than the concentration of boron ions, which have P type conductivity, the dopant concentration in channel 66 has a P type conductivity. However, in Juang, N type LDD regions 64 are formed by implanting phosphorus ions in to LDD regions 64 and, consequently, N type LDD regions 64 have N type conductivity. See, for example, column 2, lines 62-66 and Figure 6 of Juang. Thus, in Juang, N type LDD regions 64 have N type conductivity in contrast to the dopant concentration in channel 66, which has P type conductivity. Furthermore, Juang fails to teach, disclose, or suggest source and drain regions and a dopant concentration region in a channel region,

where the source and drain regions and the dopant concentration region in the channel region have a second conductivity type and a well has a first conductivity type, as specified in independent claim 3.

Moreover, Juang fails to teach, disclose, or suggest a plurality of floating gate transistors connected in series, where each floating gate transistor has a source and a drain region formed in a well of a substrate. Thus, Juang fails to remedy the basic deficiencies of Pio discussed above. Thus, neither Pio nor Juang discloses a memory array comprising a plurality of floating gate transistors connected in series and a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type.

The Examiner has stated that it would have been an obvious to modify the structure of Pio to include a dopant concentration displaced about a target region, where the target region is situated below the channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant and wherein the source and drain regions and the dopant concentration have the same conductivity, which the Examiner has stated is clearly suggested by Juang, in order to obtain proper threshold voltage and improve short-channel effect behavior. Page 3 of the Final Rejection dated September 29, 2003.

However, the Examiner has failed to provide any motivation that is disclosed or suggested in Pio or Juang to modify the structure in Pio to include the above elements, which the Examiner states as being clearly suggested by Juang. Thus, the purported combination of Pio and Juang suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Appellant's disclosure, which is impermissible.

For the foregoing reasons, Appellant respectfully submits that the present invention, as disclosed by independent claim 3, is not suggested, disclosed, or taught by Pio and Juang, either singly or in combination thereof. As such, the present invention, as defined by independent claim 3, is patentably distinguishable over Pio and Juang. Thus, claim 4 depending from independent claim 3 is, *a fortiori*, also patentably distinguishable over Pio and Juang for at least the reasons presented above. Additionally, Pio and Juang do not teach, disclose, or suggest a dopant concentration that is formed by a tilted ion implantation utilizing as a mask, at least a part of gate structure of each floating gate transistor, as specified in dependent claim 4.

B. Claims 9 and 12-14

Claims 9 and 12-14 stand rejected under 35 U.S.C. §103 over Pio in view of Juang. For the reasons discussed below, Appellant respectfully submits that the present invention, as defined by independent claim 9, is patentably distinguishable over Pio and Juang, considered singly or in combination thereof.

In contrast to the present invention as defined by independent claim 9, Pio and Juang do not teach, disclose, or suggest a transistor having a source and a drain region

formed in a well of a substrate, where a channel region separates the source and drain regions, a dopant concentration region displaced about a target region situated below the channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type.

As discussed above, Pio fails to teach, disclose, or suggest a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. Moreover, Pio fails to provide any motivation for forming a dopant concentration region displaced about a target region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the source and drain regions and the dopant concentration region have a second conductivity type.

Thus, Pio has failed to disclose a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source

and drain regions and the dopant concentration region have a second conductivity type, which are also not disclosed or suggested in Juang.

Also, as discussed above, Juang fails to teach, disclose, or suggest source and drain regions and a dopant concentration region in a channel region, where the source and drain regions and the dopant concentration region in the channel region have a second conductivity type and a well has a first conductivity type. Thus, Juang fails to cure the basic deficiencies of Pio discussed above. In other words, neither Pio nor Juang discloses a dopant concentration region displaced about a target region situated below a channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant, and where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type.

The Examiner has stated that it would have been an obvious to modify the structure of Pio to include a dopant concentration displaced about a target region, where the target region is situated below the channel region, where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant and wherein the source and drain regions and the dopant concentration have the same conductivity, which the Examiner has stated is clearly suggested by Juang, in order to obtain proper threshold voltage and improve short-channel effect behavior. Page 3 of the Final Rejection dated September 29, 2003. However, the Examiner has failed to provide any motivation that is disclosed or

suggested in Pio or Juang to modify the structure in Pio to include the above elements, which the Examiner states as being clearly suggested by Juang. Thus, the purported combination of Pio and Juang suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Appellant's disclosure, which is impermissible.

For the foregoing reasons, Appellant respectfully submits that the present invention, as disclosed by independent claim 9, is not suggested, disclosed, or taught by Pio and Juang, either singly or in combination thereof. As such, the present invention, as defined by independent claim 9, is patentably distinguishable over Pio and Juang. Thus, claims 12-14 depending from independent claim 9 are, *a fortiori*, also patentably distinguishable over Pio and Juang for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 3 and 9 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 3, 4, 9, and 12-14 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 3, 4, 9, and 12-14 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith in triplicate along with an Appendix of the appealed claim and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 4/27/04

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APPENDIX OF CLAIMS ON APPEAL

Claim 3: A memory array comprising:

a plurality of floating gate transistors connected in series,

each floating gate transistor having formed, in a well of a substrate,

a source and a drain region

and

a channel region separating said source and drain regions,

a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant;

wherein said well has a first conductivity type, said source and said drain regions have a second conductivity type, and said dopant concentration region has said second conductivity type.

Claim 4: The memory array of claim 3 wherein said dopant concentration region is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of each floating gate transistor.

Claim 9: A transistor comprising:

in a well structure of a substrate, a source and a drain region and a channel region separating said source and said regions, a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant;

wherein said well structure has a first conductivity type, said source and said drain regions have a second conductivity type, and said dopant concentration region has said second conductivity type.

Claim 12: The transistor of claim 9 wherein said dopant concentration region is provided by a tilted ion implantation utilizing as a mask, at least part of a gate structure of said transistor.

Claim 13: The transistor of claim 9, wherein the transistor is an NMOS transistor.

Claim 14: The NMOS transistor of claim 13, wherein the NMOS transistor is a floating gate transistor.